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form said buried oxide region which electrically isolates a superficial Si-containing layer from a bottom Si-containing layer, wherein said annealing reduces the number of tile or divot defects present at a top surface of said superficial Si-containing layer.

Please add new Claim 50:

50. A method of substantially reducing the number of tile or divot defects that are present in a silicon-on-insulator (SOI) substrate, said method comprising the steps of:

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(a) implanting oxygen ions into a surface of a Si-containing substrate, said implanted oxygen ions having a concentration sufficient to form a buried oxide region during a subsequent annealing step; and

(b) annealing said substrate containing said implanted oxygen ions in an ambient gas that comprises from about 0 to about 90% oxygen and from about 10 to about 100% of at least one high surface mobility gas, selected from the group consisting of H2, Kr and combinations thereof to form said buried oxide region which electrically isolates a superficial Si-containing layer from a bottom Si-containing layer, wherein said annealing reduces the number of tile or divot defects present at a top surface of said superficial Si-containing layer.

REMARKS

Favorable reconsideration and allowance of the claims of the present application, as amended herein, are respectfully requested. Before addressing the specific rejection raised in the Final Rejection dated October 22, 2002, Applicants have amended Claims 1 and 49 and have added new Claim 50.

Claims 1 and 49 have has been amended to positively recite that the annealing process step reduces the number of tile or divot defects formed in the surface of the Si-

containing layer. Support for this amendment is found throughout the present specification; i.e., Page 3, lines 25-30; Page 4, lines 11-14; Page 5, lines 17-19; Page 7, lines 1-14; and Page 12, lines 18-20. More specifically, referring to Page 12, lines 18-20, applicants disclose that "the annealing conditions reduce the number of tile or divot defects present in the superficial Si-containing layer so as to allow optical detection of any other defect that has a lower density than the tile or divot defect." Additionally, referring to FIG. 2A and related text at Page 6, line 30 – Page 7, line 14, the "superficial Si-containing layer contains fewer tiles **16** (divots) and that the tiles (divots) are much larger than in the case of the prior art tiles shown FIG 1A. Because of these two factors, a conventional optical inspection tool can detect other processing features and/or defects that are difficult to detect on prior art SOI substrates.

New Claim 50 positively recites that the annealing ambient includes from about 10% to about 100% of at least one high mobility gas that hinders oxide growth where the high mobility gas is selected from H_2, Ar and combinations thereof. Support for this newly added claim is found at Page 12, line 23 to Page 13, line 11.

Since the above amendments to the claims do not introduce any new matter into the application, entry thereof is respectfully requested. As required by 37 C.F.R. §1.121, applicants have attached a marked-up copy of amended Claims 1 and 49. The attachment is captioned as "MARKED UP VERSION SHOWING CHANGES MADE".

In the Final Rejection, Claims 1-22, 25-36, 40, and 48-49 were rejected under 35 U.S.C. §103 as allegedly unpatentable over the combined disclosures of U.S. Patent No. 6,090,689 to Sadana, et al. ("Sadana '689"), U.S. Patent No. 5,534,446 to Tachimori, et al. ("Tachimori, et al.") and U.S. Patent No. 5,930,643 to Sadana, et al. ("Sadana '643").

Applicants submit that they have unexpectedly determined that the use of an ambient gas comprising 0 to about 90% oxygen and from about 10 to about 100% of N_2 or a high mobility gas selected from the group consisting of He, Kr, H_2 and mixtures is capable of providing an SOI substrate that contains a superfacial Si-containing layer that has a *substantial reduced number of tile or divot defects* as compared to SOI substrates that are not annealed in either of the claimed gas ambients. The reduced tiles and surface divots are not formed using conventional oxidizing ambient, which include oxygen or a mixture of oxygen and Ar.

Applicants respectfully submit that the prior art references do not render the claimed methods obvious since none of the applied references teaches or suggests that an SOI substrate including a superficial Si-containing surface having a reduced number of defects and divots can be achieved by choosing the appropriate gas ambient.

Sadana '689 is defective since the applied reference does not teach or suggest a method which includes an annealing step that uses the claimed gas ambients, which applicants have unexpectedly determined provide an <u>SOI material that has a surface Si-containing layer that has a reduced number of tile or divot defects</u>. In contrast, Sadana '689 discloses annealing in an oxidizing ambient to provide a continuous buried oxide region below the surface of the device and does not address treatment of the devices surface or the reduction of divots on the device surface.

As stated above, applicants have unexpectedly determined that the use of an ambient gas comprising 0 to about 90% oxygen and from about 10 to about 100% of N_2 or a high mobility gas selected from the group consisting of He, Kr, H_2 and mixtures therefore is capable of providing an SOI substrate that contains a superfacial Si-

containing layer that has a substantial reduced number of tile or divot defects as compared to SOI substrates fabricated by annealing in an oxygen ambient or oxygen admixed with Ar.

Tachimori, et al. do not alleviate the above defects in Sadana '689 since the applied secondary reference discloses that similar results, in terms of reduction of defects in the **buried oxide layer**, can be achieved using annealing ambients such as oxygen or a mixture of oxygen and Ar, He or nitrogen. The fact that the ambients disclosed in Tachimori, et al. are capable of reducing defects in the **buried oxide region**, does not necessarily mean that the same ambients can be used to improve the surface qualitity of the Si-containing layer that lays above the buried oxide layer. Indeed, applicants have determined which ambients can be used to provide an SOI substrate having a superfacial Si-containing layer having a reduced number of tile and divot defects.

Applicants respectfully submit that in the disclosure of Tachimori, et al. there is provided many different types of annealing ambients that can be used in forming a substantially defect free buried oxide layer. The applied reference however does not provide any guidance as to which of the annealing ambients may be used for improving the quality of the top Si-containing layer of the SOI substrate. Thus, it would be necessary for one to try the various annealing ambients disclosed in Tachimori, et al. and to determine from that trail which of the various annealing ambients and conditions would perform best for improving the quality of the top Si-containing layer. Hence, in applying the disclosure of Tachimori, et al. the Examiner appears to be invoking the application of an "obvious to try" standard which is improper at law.

This standard, as apposite to the present case, has been articulated as follows:

> The admonition that "obvious to try" is not the standard under §103 has been directed mainly at two kinds of errors. In some cases, what would have been "obvious to try" would have been to vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful. (citations omitted; emphasis supplied). In re O'Farrel, 853, F2d. 894, 903, 7 USPQ 2d 1763, 1681 (Fed. Cir. 1988).

In examining the present rejection in view of the foregoing case law, it becomes clear that the disclosure of Tachimori, et al. provides absolutely "no direction as to which of many possible choices is likely to be successful" in forming a top Si-containing layer of an SOI material that contains a substantial reduced number of tile and/or divot defects. Indeed, the applied reference is not concerned with providing a high quality top Si-containing layer, but instead its main focus is providing an SOI material that has a high quality buried oxide region. There is absolutely no correlation provided in the disclosure of Tachimori, et al. that process conditions employed in forming a high quality buried oxide region can be used in forming a high quality top Si-containing layer.

Sadana '643 also does not alleviate the above defects in Sadana '689 since the applied reference also discloses that oxygen alone, or oxygen admixed with any inert gas can be employed in producing the SOI substrate. As such, the '643 patent does not differentiate which gas ambients could be employed to provide an SOI substrate having a superficial Si-containing layer having a reduced number of tile and divots defects.

Finally, it is not inherent that the number of divot or tile defects formed on the surface of the Si-containing layer can be reduced using the process steps disclosed by the applied references, including Sadana '643, Sadana '689, and Tachimori, et al. The Federal Circuit has held that inherency cannot be based on mere speculation. *See e.g., Continental Can Co. USA, Inc. v. Monsanto Co.,* 848 F.2d 1264, 1269, 20 USPQ2d 1746,

1749 (Fed. Cir. 1991) (inherency "may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.") When anticipation is based on inherency of limitations not expressly disclosed in the assertedly anticipating reference, it must be shown that the undisclosed information was known to be present in the subject matter of the reference. See *Elan Pharmaceuticals, Inc., v. Mayo Foundation for Medical Education and Research*, 304 F.3d 1221, 1228, 64 USPQ2d 1292 (Fed. Cir. 2002) (*citing Continental Can*, 948 F.2d at 1269). The <u>alleged limitation must be necessarily present so that one of ordinary skill would recognize its presence</u>. *Crown Operations International, LTD v. Solutia Inc.*, 289 F.3d 1367, 1377, 62 USPQ2d 1917 (Fed. Cir. 2002).

The court in *Elan Pharmaceuticals v. Mayo Foundation for Medical Education and Research* held that when a rejection is based on inherency of limitations not expressly disclosed in the assertedly anticipating reference, it must be shown that the undisclosed information was known to be present in the subject matter of the reference. See *Elan Pharmaceuticals, Inc., v. Mayo Foundation for Medical Education and Research*, 304 F.3d 1221, 1228, 64 USPQ2d 1292 (Fed. Cir. 2002) (*citing Continental Can*, 948 F.2d at 1269). In *Elan Pharmaceuticals* the claim limitation at issue before the court was, "wherein said polypeptide is processed to ATF-betaAPP in a sufficient amount to be detectable in a brain homogenate of said transgenic rodent". It was undisputed that the applied reference made no reference to the formation of "ATF-betaAPP". The court found that the Examiner's applied references were no more than broad teachings and were not directed to the applicants' claimed limitation. *Id. at* 1228. The referenced prior art was described as merely "an invitation to experiment with no assurances of success"

Id. Finally, the court stated that a general recitation of known procedures does not defeat the novelty of the invention as produced by the applicant.

Similar to the prior art examined in *Elan Pharmaceuticals*, the referenced prior art cited in the present Office Action does not teach or suggest all of the claimed limitations of the invention. More specifically, the referenced prior art fails to teach or suggest an annealing step which is capable of reducing the number of tile or divot defects at a top surface of said superficial Si-containing layer. "Facts asserted to be inherent in the prior art must be shown by evidence from the prior art". In re Dembiczak, 175 F.3d 949, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999) (criticizing the hindsight syndrome wherein that which only the inventor taught is used against its teacher). Neither, Tachimori, et al. nor the Sadana, et al. references teach or suggest divot defects, as recited in amended Claims 1 and 49.

Additionally, the combined references of Tachimori, et al. and the Sadana, et al. references, similar to the prior art discussed in *Elan Pharmaceuticals*, at most disclose a general recitation of procedures that were not carried out in a manner in which one of ordinary skill in the art would recognize the unexpected advantages in divot defect reduction achieved using applicants' method, recited in amended Claims 1 and 49. Therefore, in light of the holding of *Elan Pharmaceuticals,* applicants' method recited in amended Claims 1 and 49 is not obvious.

Now referring to new Claim 50. Applicants note that the applied references do not teach or suggest an annealing ambient including a high mobility gas such as H_2 or Ar. Therefore applicants submit that new Claim 50 is not obvious in view of the referenced prior art and is patentable subject matter.

In light of the standard established by the Federal Circuit, applicants respectfully request that the §103 rejection be withdrawn.

Based on the above amendments and remarks the rejection to the claims under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal of the instant rejection are respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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MARKED UP VERSION SHOWING CHANGES MADE

IN THE CLAIMS:

Please amend Claim 1 and 49 as follows:

1. (Twice amended) A method of substantially reducing the number of tile or divot defects that are present in a silicon-on-insulator (SOI) substrate, said method comprising the steps of:

(a) implanting oxygen ions into a surface of a Si-containing substrate, said implanted oxygen ions having a concentration sufficient to form a buried oxide region during a subsequent annealing step; and

(b) annealing said substrate containing said implanted oxygen ions in an ambient gas that comprises from about 0 to about 90% oxygen and from about 10 to about 100% of N_2 to form said buried oxide region which electrically isolates a superficial Si-containing layer from a bottom Si-containing layer, wherein said annealing reduces the number of tile or divot defects present at a top surface of said superficial Si-containing layer.

49. (Amended) A method of substantially reducing the number of tile or divot defects that are present in a silicon-on-insulator (SOI) substrate, said method comprising the steps of:

(a) implanting oxygen ions into a surface of a Si-containing substrate, said implanted oxygen ions having a concentration sufficient to form a buried oxide region during a subsequent annealing step; and

(b) annealing said substrate containing said implanted oxygen ions in an ambient gas that comprises from about 0 to about 90% oxygen and from about 10 to about 100% of a high mobility gas selected from the group consisting of He, Kr, H_2 and mixtures thereof to form said buried oxide region which electrically isolates a superficial Si-containing layer from a bottom Si-containing layer, wherein said annealing reduces the number of tile or divot defects present at a top surface of said superficial Si-containing layer.

Please add new Claim 50:

50. A method of substantially reducing the number of tile or divot defects that are present in a silicon-on-insulator (SOI) substrate, said method comprising the steps of:

(a) implanting oxygen ions into a surface of a Si-containing substrate, said implanted oxygen ions having a concentration sufficient to form a buried oxide region during a subsequent annealing step; and

(b) annealing said substrate containing said implanted oxygen ions in an ambient gas that comprises from about 0 to about 90% oxygen and from about 10 to about 100% of at least one high surface mobility gas, selected from the group consisting of H2, Kr and combinations thereof to form said buried oxide region which electrically isolates a superficial Si-containing layer from a bottom Si-containing layer, wherein said annealing reduces the number of tile or divot defects present at a top surface of said superficial Si-containing layer.